Engineer Trainees Recruitment in Core VLSI Engineering Domain at SoCtronics Technologies Pvt Ltd Coordinated and Conducted by VEDA IIT

Job Requirement Form

Company Name:	**SoCtronics** Technologies Pvt Ltd www.soctronics.com, A member of **VEDA IIT** consortium www.vedaiit.org
Address:	**VEDA IIT** Telangana: 2nd Floor, AYDIV IT Park, Puppalaguda, Rangareddy 500 032 Andhra Pradesh: Vidyanagar, 1st Lane & 1st Cross, Guntur 522 007
Recruitment Drive for:	Engineering candidates in Electronics/ Electrical/ Communications/ IE/ Instrumentation or M.Sc. in Electronics
Percentage Cut-off:	70% marks or equivalent for campus students who are currently pursuing final year B.Tech/BE or M. Sc. from eligible branches 65% marks or equivalent for passed out students
Salary package:	**CTC for VLSI – LD, LI, LV, PD, PV** **₹4 to 4.6 Lakhs in 1st year** after successful completion of sponsored training at VEDA IIT and based on performance in the training
Job Location:	Hyderabad/ Guntur/Noida
Terms & Conditions:	The selected candidate shall agree to work for the company for a minimum period of 3 years after joining as an Engineer Trainee (commitment period) by submitting a security agreement with a commitment amount of ₹5 Lakhs by way of legally valid instruments

Job titles and Job Description: Engineer Trainee in the 1st year and Engineer in the 2nd year

VLSI Logic Design (LD): Logic Design is the front-end activity of a chip design that involves the essentials of digital design, Verilog behavioral & RTL design

VLSI Logic Implementation(LI): Logic Implementation involves synthesis and DFT where synthesis transforms RTL design into a gate-level netlist and DFT is an innovative design technology to enable automated testing of the chip

VLSI Logic Verification(LV): Logic Verification is to develop the tests and verify the correct behavior of a given design against its specification through simulations

VLSI Physical Design (PD): Physical design is a process of converting logical connectivity of cells (netlist) into physical connectivity (manufacturable layout) meeting power, performance, and area requirements. All design components are instantiated with their geometric shapes and have appropriate routing connections in metal layers. This involves Physical Placement & Routing, Functional Equivalence, and Timing Closure

VLSI Physical Verification (PV): Physical verification is a process of verification of correct electrical and logical functionality of physical design vs logic design, manufacturability, and yield using EDA tools before the design is taped-out for semiconductor fabrication.