Engineer Trainees Recruitment

Challenging work opportunities for Graduated Engineers at

SoCtronics



in core domains

VLSI Digital Engineering

> Logic Design

RTL Design, Implementation, Verification & DFT

Physical Design

Physical Placement & Routing, Functional Equivalence, Timing Closure and Design Rule Check

VLSI Analog Engineering

Analog Design

Analog circuit design, Spice simulation and Verilog A modeling

> Custom Layout Design

Custom layout design of high performance Analog Circuits, Layout verification

Embedded System Engineering

> Embedded System Design

HW Design, Platform Engineering, Silicon Validation, Firmware/ Drivers/ Multimedia/ Application development for Mobile, Wearable and IOT systems

> Software Testing

Testing, Automation & QA for Embedded Software and Systems

VEDA Faculty positions are also available in all Domains

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Test	Eligibility: ECE/EEE/CSE in B.Tech/ M.Tech	Date & Time
Prelim.	Approved Candidates with hall tickets	26/09/15, 10 AM to 11 AM
Main	Short-listed candidates in Prelim.	26/09/15, 4 PM to 6 PM
Interview	Short-listed candidates in Main	27/09/15, 8 AM to 6 PM





Plot No. 90, Road No. 2, Banjara Hills, Hyderabad 500034, Ph: 040 - 43929999 e-mail: careers@vedaiit.com, web: www.vedaiit.org