Engineer Trainees Recruitment

Challenging work opportunities for Graduating Engineers at SoCtronics in core domains

VLSI Digital Engineering

- **Logic Design**
  RTL Design, Implementation, Verification & DFT
- **Physical Design**
  Physical Placement & Routing, Functional Equivalence, Timing Closure and Design Rule Check

VLSI Analog Engineering

- **Analog Design**
  Analog circuit design, Spice simulation and Verilog A modeling
- **Custom Layout Design**
  Custom layout design of high performance Analog Circuits, Layout verification

Embedded System Design & Engineering

- **Embedded Software Development**
  Firmware/ Drivers/ Multimedia SW/ Applications for Mobile, Wearable and IOT Systems
- **Software Testing**
  Automation, Testing & QA for Embedded SW, Systems & Applications
- **System Engineering**
  Platform Engineering, HW/Board Design, Silicon Validation/ Characterization

ELIGIBILITY : B.Tech./M.Tech./M.S./M.Sc. in Electronics/ Electrical/ Computer Science/ IT/ Instrumentation.
Final Year Students can also apply

6 months of company sponsored knowledge-intensive, industry-oriented full-time training at VEDA IIT

(One year Internship for PG students includes above training)

About VEDA

- Expert faculty from reputed VLSI Design Houses/ Institutes
- Well-equipped Labs with high-end state-of-the-art computing facilities
- Excellent placement track record in leading Technology Companies since inception
- Listed among top five institutes in VLSI Engineering by Times of India
- Innovative Teaching Company with Industry and University participation - First of its kind
- Partnership with global leaders in technology
- Pioneered in incubating many successful design teams/companies
- Associated with GLOBALFOUNDRIES collaborative University programs, exploring designs for silicon fabrication shuttle
- Lead organizers of International VLSI Conferences VLSI 2006, 2008, 2012 & 2017

Apply at www.vedaiit.org

Registration fee for B.Tech /M.Tech Pass-outs: Rs. 300/-. Last date for application : 20th Sep 2017*

No fees for campus students who apply on-line with 'valid coupon code' by 16th Sep 2017**

* Application submission can be closed earlier than this whenever the number of applicants exceeds the actual seating capacity at the exam center

** VEDA IIT provides 'valid coupon codes' to TPO/HODs of different colleges on request; Number will be limited to the seating capacity

Test	Eligibility	Date & Time
Prelim.	Approved Candidates with hall tickets	23/09/17, 9 AM to 10 AM
Main	Short-listed candidates in Prelim	23/09/17, 4 PM to 6 PM
Interview	Short-listed candidates in Main	24/09/17, 9 AM to 7 PM

Pre-placement Talk - 23/09/17, 10:15 AM to 10:45 AM

VEDA® Learn. Explore. Excel.

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