VEDA

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RECRUITMENT OF ASST. PROFESSORS

HYDERABAD & AMARAVATI

Job Description: Teaching, Research & Training

Eligibility: BE/B.Tech. & ME/M.Tech./MS in relevant branch (ECE/EEE/EIE) with 1st class or equivalent either in BE/B.Tech. or ME/M.Tech./MS.
Preference will be given to IIT/NIT graduates.
No screening test for teachers with minimum 10 years of experience.

Salary: Negotiable

Core Domains

VLSI Digital Engineering

Logic Design
Digital Design, RTL Implementation, Verification, Synthesis, DFT & Emulation

Physical Design
Physical Placement & Routing, Functional Equivalence, Timing Closure and Design Rule Check

VLSI Analog Engineering

Analog Design
Analog circuit design, Spice simulation and Verilog A modeling

Custom layout design
Analog/Custom circuit layout, Layout verification

Embedded System Design

Embedded Software, Firmware, Drivers and Applications Development, HW/Board Design, Silicon Validation & Characterization

Programming

Program development in
Unix, C, C++, PERL, TCL, Java, Data Structures

The selected candidates will be provided 6 months of knowledge intensive, industry-oriented full-time training based on requirement.

ABOUT VEDA

- Since 1997
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- Consortium Companies
- MoU with JNTUH, JNTUK

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Last date to Apply/ Send resumes: 25th June 2018

Screening Test (in choosen core domain): 30th June 2018 | 10:00 AM to 01:00 PM

Interview: Successful candidates in screening test & shortlisted experienced teachers will be called for interview.

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