

Junior Engineer Trainees Recruitment Challenging opportunities for Polytechnic Diploma Holders

VLSI Design & Engineering

Logic Design

RTL Design, Implementation, Verification, DFT & Emulation

Physical Design

Physical Placement & Routing, Functional Equivalence, Timing Closure and Design Rule Check

Custom Layout Design

Custom layout design of high performance Analog Circuits, Layout verification

Embedded System Design & Engineering

Embedded Software Development

Firmware/ Drivers/ Multimedia SW for Embedded Devices, Systems & Solutions

Software Testing

Automation, Testing & QA for Embedded SW, Systems & Applications

System Engineering

Platform Engineering, HW/Board Design, Silicon Validation/ Characterization

ELIGIBILITY

Diploma in Electronics/ Electrical/ Communications/ IE/ Computer Science/ Instrumentation

Final year students can also apply.

About VEDA

- Expert faculty from reputed VLSI Design Houses/ Institutes.
- Well-equipped Labs with high-end state-of-the-art computing facilities.
- Excellent placement track record in leading Technology Companies since inception.
- Listed among top five institutes in VLSI Engineering by Times of India.
- Innovative Teaching Company with Industry and University participation - First of its kind.
- Pioneered in incubating many successful design teams/ companies.
- Associated with GLOBALFOUNDRIES collaborative university programs, exploring designs for silicon fabrication shuttle.
- Lead organizers of International VLSI & Embedded System Design Conferences VLSI 2006, 2008, 2012 & 2017

**6 months Company sponsored
knowledge-intensive, industry oriented full-time training at VEDA IIT
(with stipend payment)**

APPLY AT www.vedaiit.org

Registration fee for Pass-outs: Rs. 300/-

Last date for application : **26th Dec 2018***

No fees for campus students who apply on-line with
'valid coupon code'** by **22nd Dec 2018**

*Application submission can be closed earlier than this whenever the number of applicants exceeds the actual seating capacity at the exam center

** VEDA IIT provides 'valid coupon codes' to TPO/HODs of different colleges on request; Number will be limited to the seating capacity

Prelim.	Approved candidates with hall tickets	29/12/18, 9 AM to 10 AM
Main	Short-Listed candidates in Prelim.	29/12/18, 3.30 PM to 5.30 PM
Interview	Short-Listed candidates in Main	30/12/18, 8.30 AM to 7 PM [#]

Pre-placement Talk - 29/12/18, 10:15 AM to 10:45 AM

[#]Interview schedule beyond this date will be intimated on that day



VEDA IIT, a unit of The VEDA Educational Society

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